Client's ref.: NTC-91021 File: 0548-8070US/final

## What is claimed is:

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- A stacked gate flash memory cell, comprising: 1
- a substrate having a cell trench and two adjacent 2 isolation trenches therein, the cell trench having two substrate sides and two isolation sides contacting the adjacent isolation 5 trenches, the isolation trench having two substrate sides and one cell side contacting the adjacent cell trench; 8
  - a bottom insulating layer disposed on the bottom of the cell trench;
  - a pair of tunnel oxide layers, each disposed on the substrate side of the cell trench and the bottom insulating layer;
  - a pair of floating gates, each disposed on the substrate side of the cell trench and covering the tunnel oxide layer;
  - a conformal inter-gate dielectric layer overlying the layers tunnel oxide and the bottom insulating layer;
  - a control gate overlying the inter-gate dielectric layer in the cell trench; and
- two pairs of source/drain regions, each respectively 22 disposed on the same substrate side of each 23 isolation trench. 24
- The cell as claimed in claim 1, wherein the 2. 1 substrate is a P-type silicon substrate.

## /Shawn/Kevin revised

- 3. The cell as claimed in claim 1, wherein the bottom insulating layer is silicon dioxide.
- 1 4. The cell as claimed in claim 1, wherein the tunnel oxide layer is silicon dioxide.
- 5. The cell as claimed in claim 1, wherein the floating gate and the control gate are N-type dopant doped polysilicon.
- of. The cell as claimed in claim 1, wherein the inter-gate dielectric layer is silicon dioxide.
- 7. The cell as claimed in claim 1, wherein the isolation trench is filled with an insulating material comprising silicon dioxide.